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(57) Abstract :
A circuit includes a degeneration p channel metal oxide semiconductor (PMOS) transistor (102) a load PMOS transistor (104) and a clamp transistor (110) configured to clamp a voltage applied to a resistance based memory element (112) during a sensing operation. A gate of the load PMOS transistor is controlled by an output of a not AND (NAND) circuit (106).

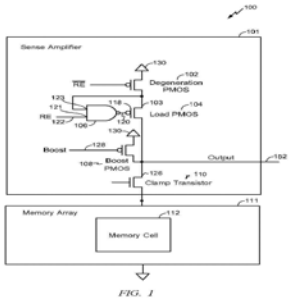

FIG. 1

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