

(54) Title of the invention : STRESS AWARE DESIGN FOR INTEGRATED CIRCUITS

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(57) Abstract :

A method of circuit design involving an integrated circuit (IC) having an interposer can include identifying an active resource implemented within the IC (200 500) within a zone (465 470 535) of the interposer (205 505) exposed to an amount of stress that exceeds a normalized amount of stress on the interposer and selectively assigning an element of the circuit design to be implemented within the IC to the active resource according to a stress aware analysis of the circuit design as implemented within the IC. Another zone (620) is characterized by a substantially normalized stress throughout the other zone.

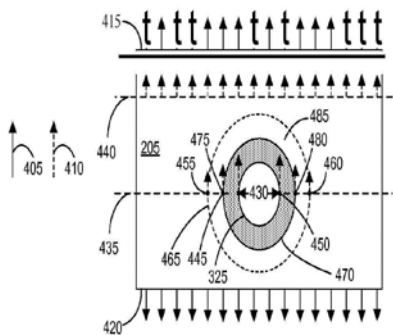


FIG. 4

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